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EXAMINER
ROJAS, DANIEL E

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 February 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-16</u> is/are pending in the application.

    4a) Of the above claim(s) <u>9 and 10</u> is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-8 and 11-16</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>03 February 2006</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☒ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>2/22/2007 and 2/3/2006</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____ .

DETAILED ACTION

Election/Restrictions

1.   During a telephone conversation with Samuel Borodach on May 3, 2008 a
provisional election was made without traverse to prosecute the invention of Species 1,
claims 1-8 and 11-16. Affirmation of this election must be made by applicant in replying
to this Office action. Claims 9 and 10 are withdrawn from further consideration by the
examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. Applicant is
reminded that upon the cancellation of claims to a non-elected invention, the
inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the
currently named inventors is no longer an inventor of at least one claim remaining in the
application. Any amendment of inventorship must be accompanied by a request under
37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

2.   Acknowledgment is made of applicant's claim for foreign priority based on an
application filed in Japan on 8/8/2003. It is noted, however, that applicant has not filed
a certified copy of the 2003-290229 application as required by 35 U.S.C. 119(b).

Drawings

3.   Figures 8-10 should be designated by a legend such as --Prior Art-- because
only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in
compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid
abandonment of the application. The replacement sheet(s) should be labeled
"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office

action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4.   Claims 1, 2, 4, and 6 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. The terms "substantially one-half" and

"substantially equal" do not define a specific amount of acceptable variance (for

example, "within 0.5V of half of the supply voltage").

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
        obviousness or nonobviousness.

7.   Claims 1-8 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Higuchi et al (US Patent No. 5,053,646), hereinafter referred to as Higuchi.

8.   For claim 1, Higuchi teaches in Figure 6 a circuit which comprises a three-state

inverter (comprised of 41, 42, 43, and 44) that switches the output thereof among three

states, namely a high, a low, and a high-impedance state (as explained below); and

an inverter (40) but fails to teach that the three-state inverter has a threshold voltage

with reference to which the three-state inverter evaluates an input thereto to determine

whether or not to change a state of an output thereof is equal to substantially one-half of

a supply voltage fed in and that the inverter of which a threshold voltage with reference

to which the inverter evaluates an input thereto to determine whether or not to change a

state of an output thereof is equal to substantially one-half of the supply voltage fed in.

However, it would have been obvious to one of ordinary skill in the art at the time of

invention to set the threshold voltage of both the said three-state inverter and the said

inverter to substantially one half of the supply voltage fed in since it has been held that

discovering an optimum value of a result effective variable involves only routine skill in

the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

9.   For claim 2, Higuchi further teaches that one of the logic gates is a two-input,

one-output AND gate (as explained below) comprising: a first three-state inverter

(41,42, 43, 44) of which an input terminal (a) serves as one input of the AND gate; a

second three-state inverter (45, 46, 47, 48) of which an input terminal (b) serves as

another input of the AND gate and of which the input terminal is connected to a state

control terminal thereof (as explained below), the second three-state inverter

determining whether or not to bring an output thereof into a high-impedance state

according to a state of a signal fed to the state control terminal thereof (inherent based

on the structure of Higuchi); a first inverter (40) of which an input terminal is connected

to a node between output terminals of the first and second three-state inverters, and of

which an output terminal serves as an output of the AND gate; and a second inverter

(49) of which an input terminal is connected to the input terminal of the second three-

state inverter (in parallel, as shown), and of which an output terminal is connected to the

state control terminal of the first three-state inverter (gate of 44) but fails to teach that

the threshold voltages of the first and second three-state inverters and of the first and

second inverters are substantially equal to one-half of the supply voltage fed in.

Higuchi's circuit is capable of functioning as a two input, one output AND gate wherein

input "a" is set to a logic low (i.e. wherein "a" is held at a constant, logic low value).

Each of the input terminals of an AND gate can be considered a state control terminal

since it directly affects the output of the AND gate. It would have been obvious to one

of ordinary skill in the art at the time of invention to set the threshold voltage of both the

said first and second three-state inverters and the said first and second inverters to

substantially one half of the supply voltage fed in since it has been held that discovering

an optimum value of a result effective variable involves only routine skill in the art. In re

Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

10.   For claim 3, the modified version of Higuchi as defined above teaches the circuit

of claim 2 but fails to teach that the first inverter is a three-state inverter of which a state

control terminal is grounded. However, a three state inverter of which a state control

terminal is grounded operates in the same way as a push-pull inverter (i.e. a PMOS

transistor with a gate connected to an input, drain connected to the output and source

connected to the supply voltage and an NMOS transistor with a gate connected to the input, drain connected to the output and source connected to ground). Therefore, it would have been obvious to one of ordinary skill in the art to replace Higuchi's inverter with a three state inverter of which a state control terminal is grounded because the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of invention.

11.   For claim 4, Higuchi further teaches a two-input, one-output OR gate (as explained below) comprising: a first three-state inverter of which an input terminal serves as one input of the OR gate (a), and that receives at a state control terminal thereof another input to the OR gate (c_i), the first three-state inverter determining whether or not to bring an output thereof into a high-impedance state according to a state of a signal fed to the state control terminal thereof (inherent based on the structure of Higuchi, as further defined below); a second three-state inverter of which an input terminal serves as another input of the OR gate (b); a first inverter (40) of which an input terminal is connected to a node between output terminals of the first and second three-state inverters, and of which an output terminal serves as an output of the OR gate; and a second inverter (49) of which an input terminal is connected to the input terminal of the second three-state inverter (since they are receiving the same signal, they are inherently electrically connected, as further explained below), and of which an output terminal is connected to the state control terminal of the second three-state inverter (as shown), but fails to teach that the threshold voltages of the first and second three-state inverters and of the first and second inverters are substantially equal to one-half of the

supply voltage fed in. A three input, one output OR gate inherently comprises two

inputs and one output. Higuchi's circuit is capable of functioning as an OR gate when

inputs a and b and c_i receive the same signal. It would have been obvious to one of

ordinary skill in the art at the time of invention to set the threshold voltage of both the

said first and second three-state inverters and the said first and second inverters to

substantially one half of the supply voltage fed in since it has been held that discovering

an optimum value of a result effective variable involves only routine skill in the art. In re

Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

12.   For claim 5, the modified version of Higuchi as defined above teaches the circuit

of claim 4 but fails to teach that the first inverter is a three-state inverter of which a state

control terminal is grounded. However, a three state inverter of which a state control

terminal is grounded operates in the same way as a push-pull inverter (i.e. a PMOS

transistor with a gate connected to an input, drain connected to the output and source

connected to the supply voltage and an NMOS transistor with a gate connected to the

input, drain connected to the output and source connected to ground). Therefore, it

would have been obvious to one of ordinary skill in the art to replace Higuchi's inverter

with a three state inverter of which a state control terminal is grounded because the

substitution of one known element for another would have yielded predictable results to

one of ordinary skill in the art at the time of invention.

13.   For claim 6, Higuchi further teaches that one of the logic gates is a logic gate that

selects and outputs one of two clocks according to a select signal fed thereto, the logic

gate comprising: a first three-state inverter (41,42, 43, 44) that receives at an input

terminal thereof one clock (a), and that receives at a state control terminal thereof the

select signal (c_i), the first three-state inverter determining whether or not to bring an

output thereof into a high-impedance state according to a signal fed to the state control

terminal thereof (inherent based on the structure of Higuchi); a second three-state

inverter (45,46,47,48) that receives at an input terminal thereof another clock (b); a first

inverter (40) of which an input terminal is connected to a node between output terminals

of the first and second three-state inverters, and of which an output terminal serves as

an output of the logic gate; and a second inverter (49) that receives at an input terminal

thereof the select signal, and of which an output terminal is connected to the state

control terminal of the second three-state inverter but fails to teach that the threshold

voltages of the first and second three-state inverters and of the first and second

inverters are substantially equal to one-half of the supply voltage fed in. It would have

been obvious to one of ordinary skill in the art at the time of invention to set the

threshold voltage of both the said first and second three-state inverters and the said first

and second inverters to substantially one half of the supply voltage fed in since it has

been held that discovering an optimum value of a result effective variable involves only

routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

14.   For claim 7, the modified version of Higuchi as defined above teaches the circuit

of claim 6 but fails to teach that the first inverter is a three-state inverter of which a state

control terminal is grounded. However, a three state inverter of which a state control

terminal is grounded operates in the same way as a push-pull inverter (i.e. a PMOS

transistor with a gate connected to an input, drain connected to the output and source

connected to the supply voltage and an NMOS transistor with a gate connected to the

input, drain connected to the output and source connected to ground). Therefore, it

would have been obvious to one of ordinary skill in the art to replace Higuchi's inverter

with a three state inverter of which a state control terminal is grounded because the

substitution of one known element for another would have yielded predictable results to

one of ordinary skill in the art at the time of invention.

15.   For claim 8, Higuchi further teaches that the three-state inverter comprises:

a first transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

16.   For claim 11, the modified version of Higuchi as defined above teaches a first

transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

17.   For claim 12, the modified version of Higuchi as defined above teaches a first

transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

18.   For claim 13, the modified version of Higuchi as defined above teaches a first

transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

19.   For claim 14, the modified version of Higuchi as defined above teaches a first

transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

20.   For claim 15, the modified version of Higuchi as defined above teaches a first

transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

21.   For claim 16, the modified version of Higuchi as defined above teaches a first

transistor (42) that receives at a first electrode thereof the supply voltage (source

terminal via transistor 41); a second transistor (41) of which a first electrode (source

terminal) is connected to a second electrode (drain terminal, via the source) of the first

transistor, and that is of a same conductivity type as the first transistor (PMOS, as

shown); a third transistor (44) of which a second electrode (drain terminal) is connected

to a second electrode of the second transistor (drain terminal), and that is of an opposite

conductivity type to the first transistor (NMOS, as shown); a fourth transistor (43) of

which a second electrode (drain terminal) is connected to a first electrode (source

terminal) of the third transistor, of which a first electrode is grounded (via transistor 44),

and that is of an opposite conductivity type to the first transistor (NMOS); and an

inverter (49) of which an output terminal is connected to a control electrode of the third

transistor (44), wherein a node between control electrodes of the first and fourth

transistors serves as an input terminal of the three-state inverter (terminal at which a is

applied), a node between the second electrodes of the second and third transistors

serves as an output terminal of the three-state inverter (the node connected to the input

of 40), and a node between a control electrode of the second transistor and an input

terminal of the inverter serves as a state control terminal of the three-state inverter (as

shown).

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-

5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate

Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816